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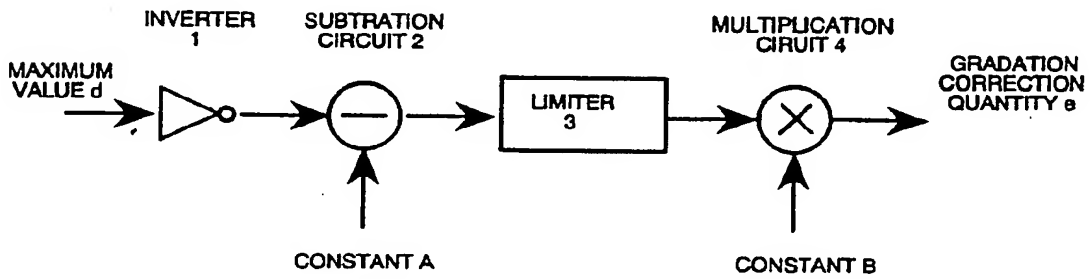
## (54) Gain control circuit and gradation correcting apparatus.

(57) A small scale gain control circuit for controlling gain correction quantity is realized, using the configuration of an inverter (1), a subtraction circuit (2), a limiter (3), and a multiplication circuit (4). Gain correction quantity is controlled in such a way that in the gradation correcting apparatus a first constant fixes a value beyond which gain correction quantity is zero and a second constant fixes an inclination of the characteristics line.

*FIG. 3*

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## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a gradation correcting apparatus and specifically to a gradation correcting apparatus for use in television receivers, video tape recorders, and video projectors. In particular, a gain control circuit for controlling the quantity of correction applied an input image in order to automatically adjust that image is disclosed.

### Description of the Prior Art

A gradation correcting apparatus automatically acts on a video gradation signal (which includes information such as picture brightness and pitcure contrast) to obtain a television picture with optimum contrast. With the recent trend towards high quality television receivers, such devices have received much attention.

A gradation correcting apparatus typically includes a gain control circuit in order to control correction quantity.

A conventional gradation correcting apparatus, including a gain control circuit, is explained with reference to the block diagram shown in Figure 1.

The gradation correcting apparatus comprises: a histogram memory 5 for representing brightness distribution of an input brightness signal; a look up table (LUT) arithmetic circuit 6 for performing accumulative addition of frequency in the histogram, and thereafter normalizing each accumulative frequency as described later; a look up table memory 7 for storing the normalized accumulative frequency supplied from the LUT arithmetic circuit 6 and supplying a correction quantity in response to the brightness level of the input brightness signal; a maximum value detecting circuit 8 for detecting the maximum value of difference between adjacent normalized accumulative frequencies in the LUT arithmetic circuit 6; a gain control circuit 9 for supplying correction quantity in response to the maximum value of difference in the maximum value detecting circuit 8; and a multiplication circuit 10 for multiplying an output of the LUT memory 7 by an output of the gain control circuit 9 and sending a gradation correcting signal.

Operation of the gradation correcting apparatus will now be explained with reference to Figures 2a - e, in which each characteristic graph shows a step in the consecutive conversion of a brightness signal within the gradation correcting apparatus. For purposes of this explanation, it is assumed that an input brightness signal is valued in 256 gradations as expressed by 8-bit binary scale.

First, a brightness distribution of the input brightness signal **a** is obtained. This brightness distribution is obtained through a horizontal sweep which comprises a train of pixels. The brightness of each pixel or each sampled pixel is measured and classified into 256 brightness grades. The frequency of each brightness grade may be counted and presented in the form of a histogram as shown in Figure 2(a). This brightness distribution is stored in the histogram memory 5. The contents of the memory 5 are cleared off and the memory 5 is set to zero once every one vertical scaming duration (or integer multiple thereof).

Next, the LUT arithmetic circuit 6 (which may include, for example, an arithmetic logic unit or a microprocessor) conducts the accumulative addition of frequency in the histogram, calculates the normalization coefficient such that the maximum accumulative frequency as obtained in the last accumulative addition is equal to the maximum value 256, and multiplies each accumulative frequency by the multiplication coefficient, as shown in Figure 2(b).

The result **b** of the preceding procedure is stored in the LUT memory 7.

Whenever an input brightness signal **a** is received by the LUT memory 7, a correction signal **c** is transmitted therefrom. The value of the correction signal **c** is given by the algorithmic operation such that correction value equals (normalized accumulative frequency (dimensionless) minus input brightness value (dimensionless)), thus leading to the characteristic graph as shown in Figure 2(c). This graph provides for correction of picture brightness such that lower brightness level are reduced while higher brightness level are increased. In other words, this graph provides for enhanced contrast.

Put another way, **c** - **b** (the accumulative addition of frequency) - 45° line of accumulative addition of frequency. Alternatively, correction signal **c** is the difference between an input image and an image having ideal gradation.

By means of the maximum value detecting circuit 8, the maximum value of difference **d** between adjacent normalized accumulative frequencies as indicated in Figure 2(b) is detected, and sent to the gain control circuit 9.

Next, by means of the gain control circuit 9, the maximum value of difference **d** is converted to a value of a gain correction signal **e** according to the characteristic graph shown in Figure 2(d), which is obtained by expertise of this art. The more concentrated the input brightness values are in a certain brightness level, the larger the maximum value of difference **d** becomes. The graph shown in Figure 2(d) indicates that in the case of concentrated input brightness values, the value of the gain correction signal **e** has to be reduced.

The gain correction signal **e** transmitted from the gain control circuit 9 determines the resultant gain of the multiplication circuit 10 as the value of the gain correction signal divided by the number 256. For example, when the value of the gain correction value is

128, the gain is 1/2, thus the value of the outgoing signal, i.e., a gradation correction signal **f**, becomes half the value of the incoming signal, i.e., the correction signal **c**. The plot of the value of the gradation correction signal **f** against the value of the input brightness signal **a** is shown in Figure 2(e). Correction signal **f** is added to the input brightness signal **a** at the addition circuit 11, resulting in the corrected brightness signal **a**.

The gain control circuit 9 includes a read only memory (ROM), and the characteristic as shown in Figure 2(d) is written into the ROM.

The gain control circuit 9 transmits the gain correction signal **e** upon receipt of the maximum value of difference **d**.

Unfortunately, gain control circuits incorporating a ROM are complex and large. This results in a large PC board and a high cost.

## SUMMARY OF THE INVENTION

A gain control circuit according to the present invention comprises: an inverter for inverting an input signal; a subtraction circuit for subtracting the first constant from an input signal; a limiter for passing an input signal when it is not less than zero, and stopping it when it is otherwise; and a multiplication circuit for multiplying a signal by the second constant.

In the above-mentioned configuration, according to the present invention, gradation correction control is easily realized in such a way that when a variable exceeds a value specified by the first constant, the variable is set to zero by the limiter, and when it is not more than the first constant it varies in the way specified by the second constant, thus sending a gain control signal.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a gradation correction apparatus including a conventional gain control circuit.

Figures 2a - e are a set of graphs for explaining the function of a conventional apparatus.

Figure 3 is a block diagram of an exemplary embodiment of a gain control circuit in accordance with the present invention.

Figure 4 is a graph for explaining the function of an embodiment of a gain control circuit in accordance with an exemplary embodiment of the present invention.

Figure 5 is a graph for illustrating how the linear characteristics of the present invention approximately coincide with a portion of the characteristic curve of the prior art.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

An exemplary embodiment of a gain control circuit in accordance with the present invention is now explained. Figure 3 is a block diagram of the gain control circuit comprising: an inverter 1 for inverting a signal, a subtraction circuit 2 for subtracting the first constant **A** from an input signal, a limiter 3 for sending zero signal if an input signal is less than zero, and a multiplication circuit 4 for multiplying an input signal by the second constant **B**.

In this configuration, the function of the gain control circuit is now explained.

First, a signal indicative of the maximum value of difference **d** as previously defined in the histogram of normalized accumulative frequency versus input brightness level is transmitted to the inverter 1. Then, the output signal from the inverter 1 is transmitted to the subtraction circuit 2, being subtracted from by the first constant **A**.

Next, the output signal from the subtraction circuit 2 is transmitted to the limiter 3, transmitting an output signal of zero when the input signal is less than zero, or passing the signal with no modification when the signal is no less than zero. Then, the output signal from the limiter 3 is multiplied by the second constant **B** by the multiplication circuit 4, thus sending a gain correction signal **e**.

The characteristic of gain correction quantity versus maximum value as obtained in the preceding procedure is shown in Figure 4.

In the above description, the constants **A** and **B** are determined so as to get an optimum correction by expertise of this art.

In Figure 4, a line **a** when the constant **A** is zero, and the constant **B** is 1 is obtained. A line **b** with an inclination of 1/2 when **A** is zero and **B** is 1/2 is also obtained. Furthermore, a line **c** when **A** is 128 and **B** is 1 is obtained. A line **d** with an inclination of 1/2 when **A** is 128 and **B** is 1/2 is obtained as well. In the range that a maximum value **d** is more than 128 in the last two cases, a horizontal zero line is obtained. For example, to keep gain correction quantity zero in the range a maximum value is more than 192, the constant **A** is desirably fixed to 64.

In this manner, as shown in Figure 5, constant **A** and constant **B** are determined such that the linear characteristics approximately coincide with a portion of the characteristic curve of the prior art.

By means of the above-mentioned procedure, gain correction quantity in the gradation correcting apparatus is controlled. This is accomplished through use of the first constant which sets a value beyond which gain correction value is zero and through the use of the second constant which determines an inclination of the line in the characteristic shown in Figure 4.

As described in the exemplary embodiment of the present invention, gain correction quantity in the gradation correcting apparatus can be realized on a smaller scale and easily put into practice by means of the gain control circuit comprising an inverter, a subtraction circuit, a limiter, and a multiplication circuit, with the first constant which fixes a value beyond which gain correction quantity is zero and the second constant which fixes an inclination of the line as drawn in Figure 4.

## Claims

1. A gain control circuit for use with a video signal and comprising:
   means for subtracting a signal representative of a first constant from said video signal to generate a subtracted signal,
   a limiter means for generating (1) an output signal of zero value when said subtracted output signal is less than zero, and (2) an output signal equal in value to said subtracted output signal when said subtracted output signal is not less than zero, and
   a multiplication circuit for multiplying said output signal by a second constant.

2. A gain control circuit as claimed in claim 1, wherein said gain control circuit is incorporated into a gradation correction apparatus.

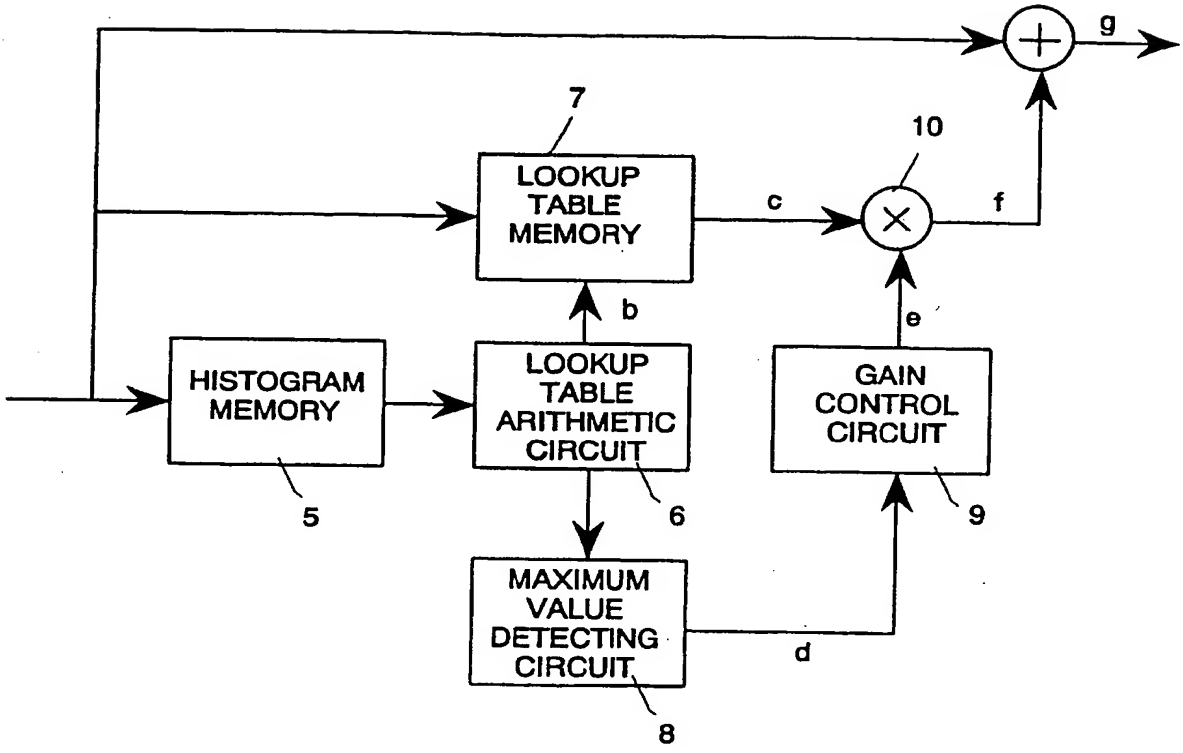



*FIG. 1*

*FIG. 2*

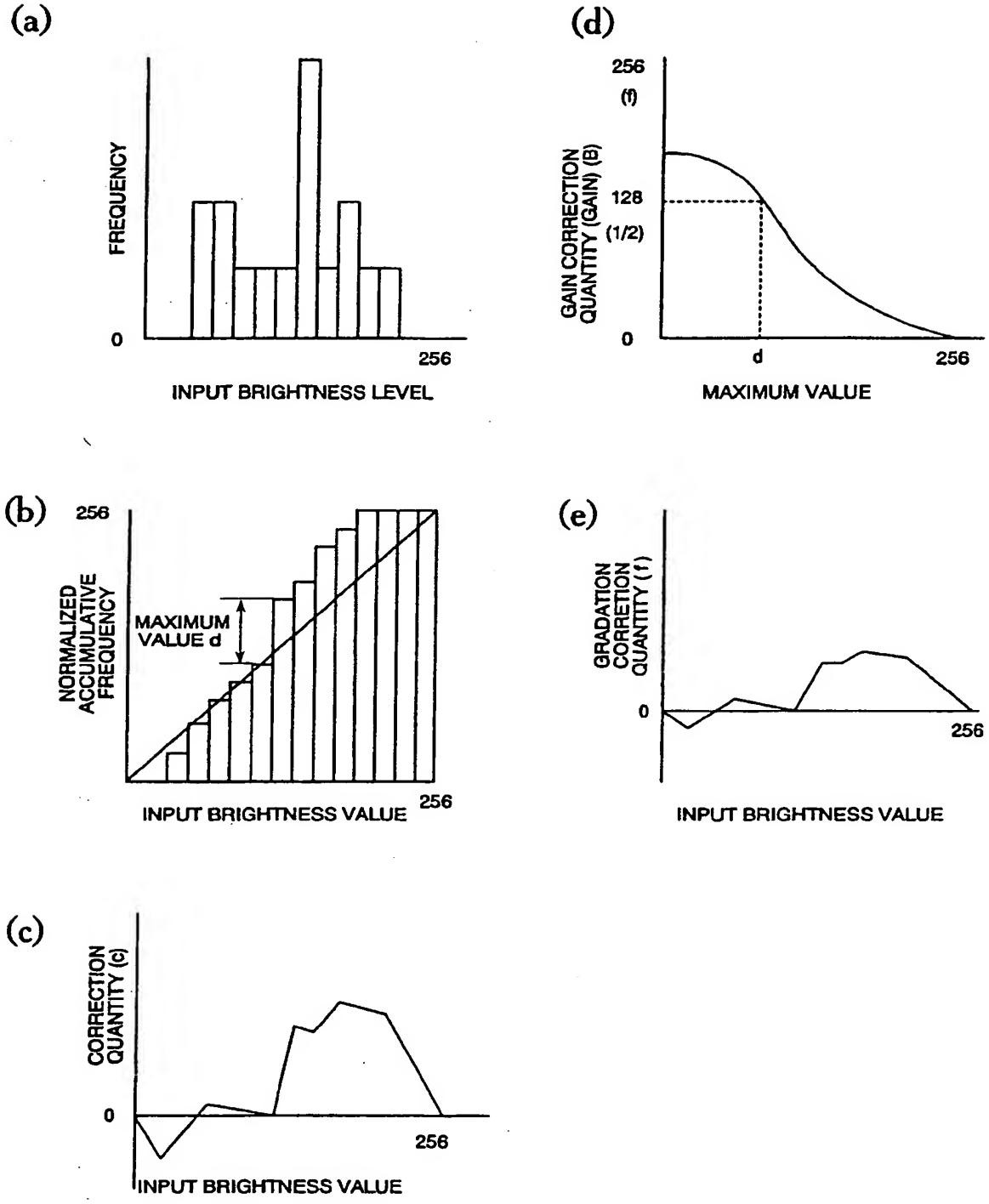


*FIG. 3*

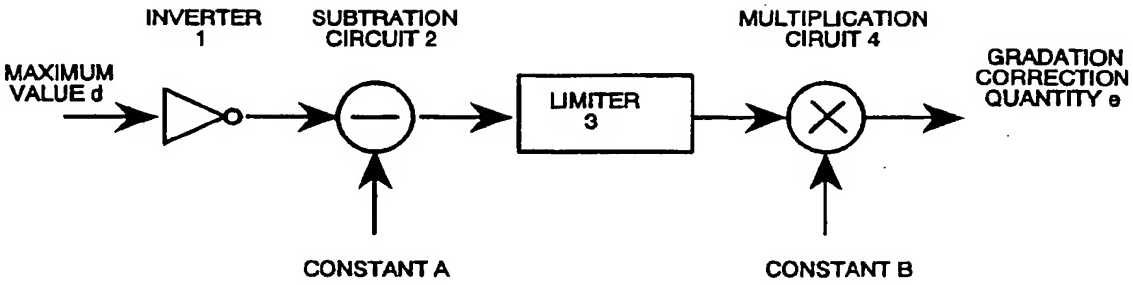
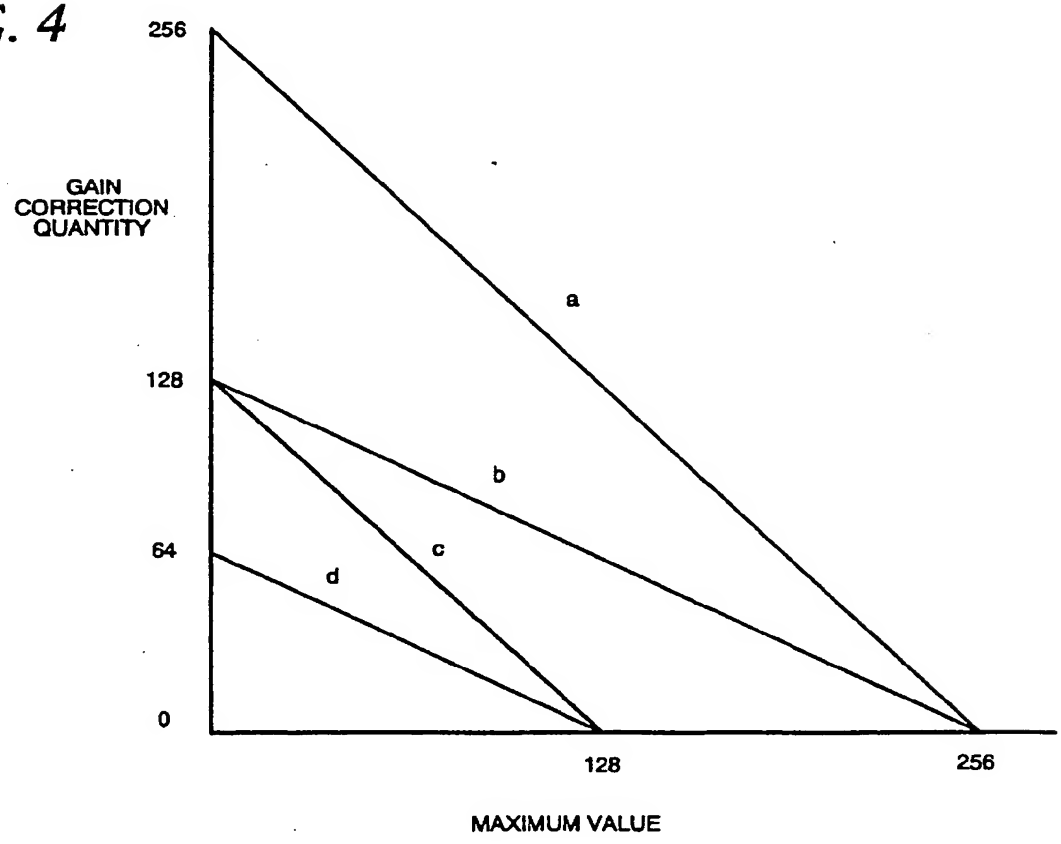



*FIG. 4*



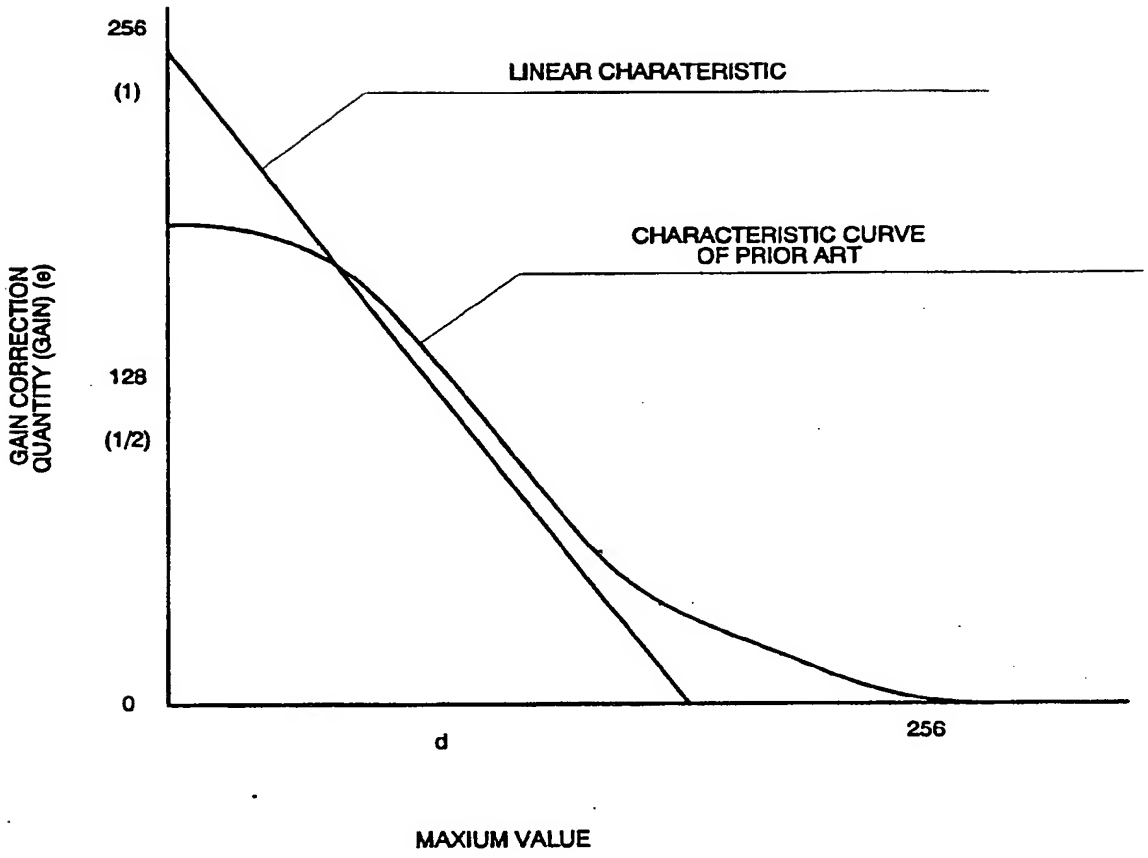



*FIG. 5*

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# EUROPEAN SEARCH REPORT

Application Number
EP 93 10 1851

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | WIRELESS WORLD<br>vol. 79, no. 1458, December 1973, HAYWARDS HEATH GB<br>pages 611 - 613<br>BRUSH ET AL. 'Contrast Expansion Processor'<br>* page 611, middle column, line 12 - page 613, middle column, line 15; figure 2 * | 1,2 | H04N5/20 |
| A | US-A-4 187 519 (VITOLS ET AL.)<br>* figure 1 * | 1,2 | |
| A | EP-A-0 235 042 (THOMSON-CGR)<br>* figures 3A-D * | 1,2 | |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 14, no. 163 (E-910)29 March 1990<br>& JP-A-20 19 070 ( TOSHIBA ) 23 January 1990<br>* abstract * | 1,2 | |
| | | | TECHNICAL FIELDS SEARCHED (Int. Cl.5)<br>H04N |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 08 JUNE 1993 | BERWITZ P. |

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